Low-cost, High-speed Parallel FIR Filters for RFSoC Front-Ends Enabled by CλaSH

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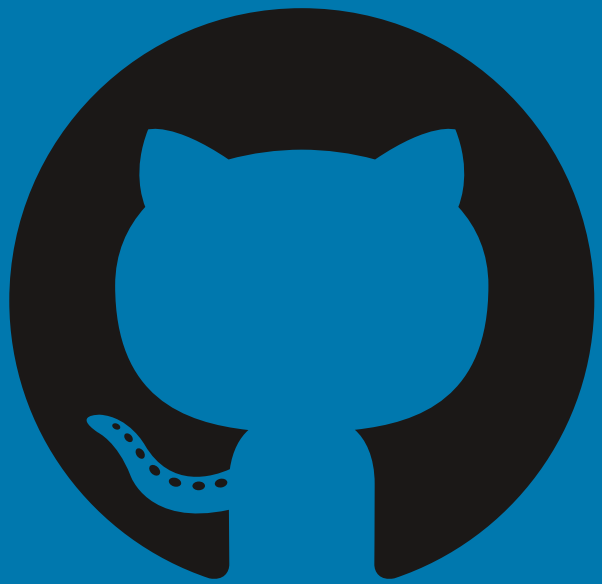
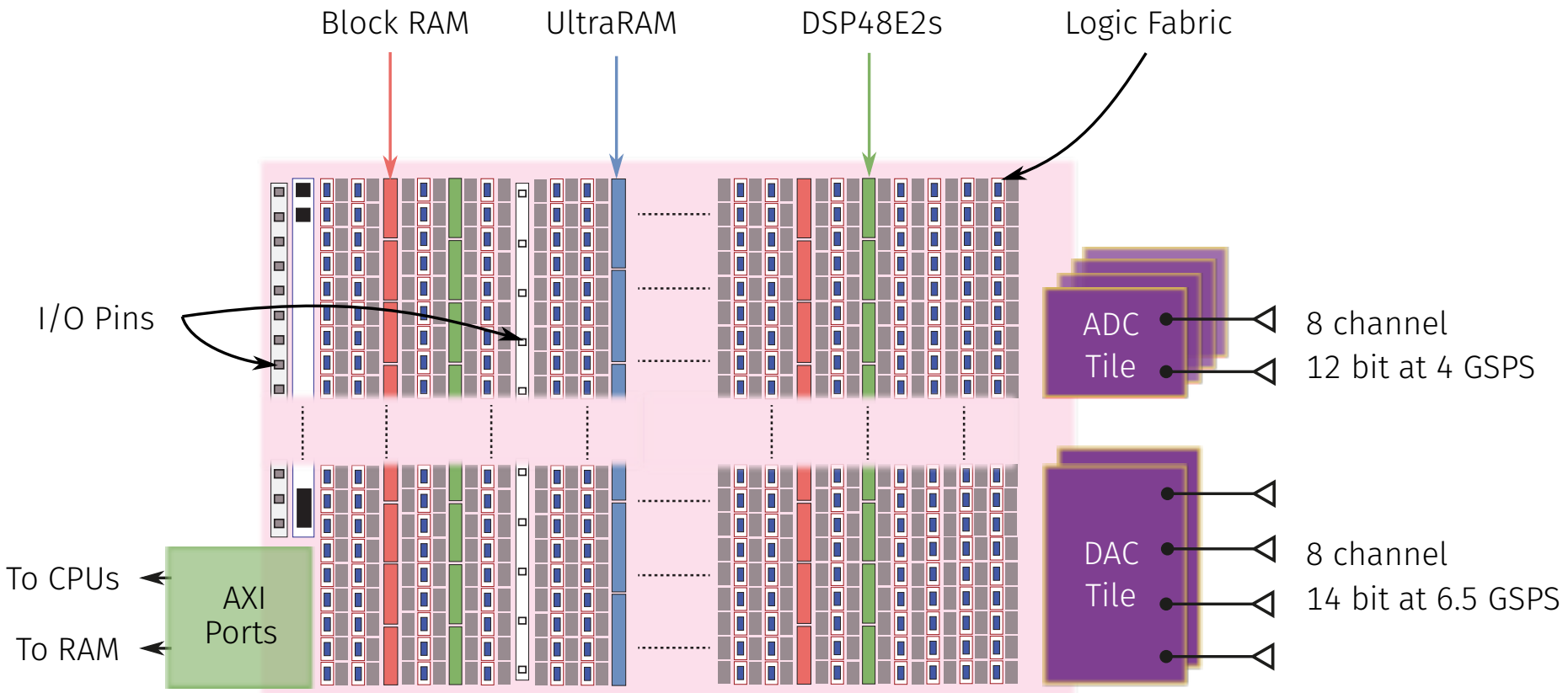


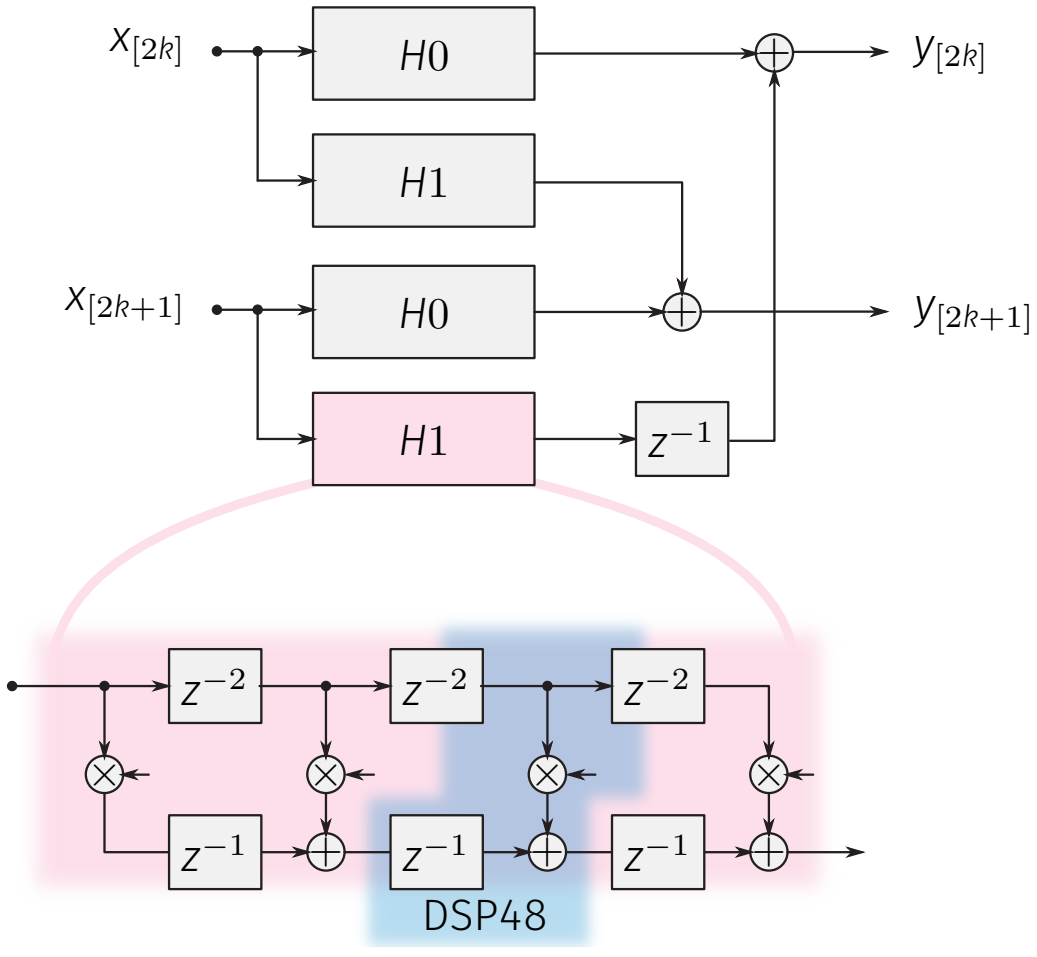
github.com/cramsay/
conifer

RFsoC Overview

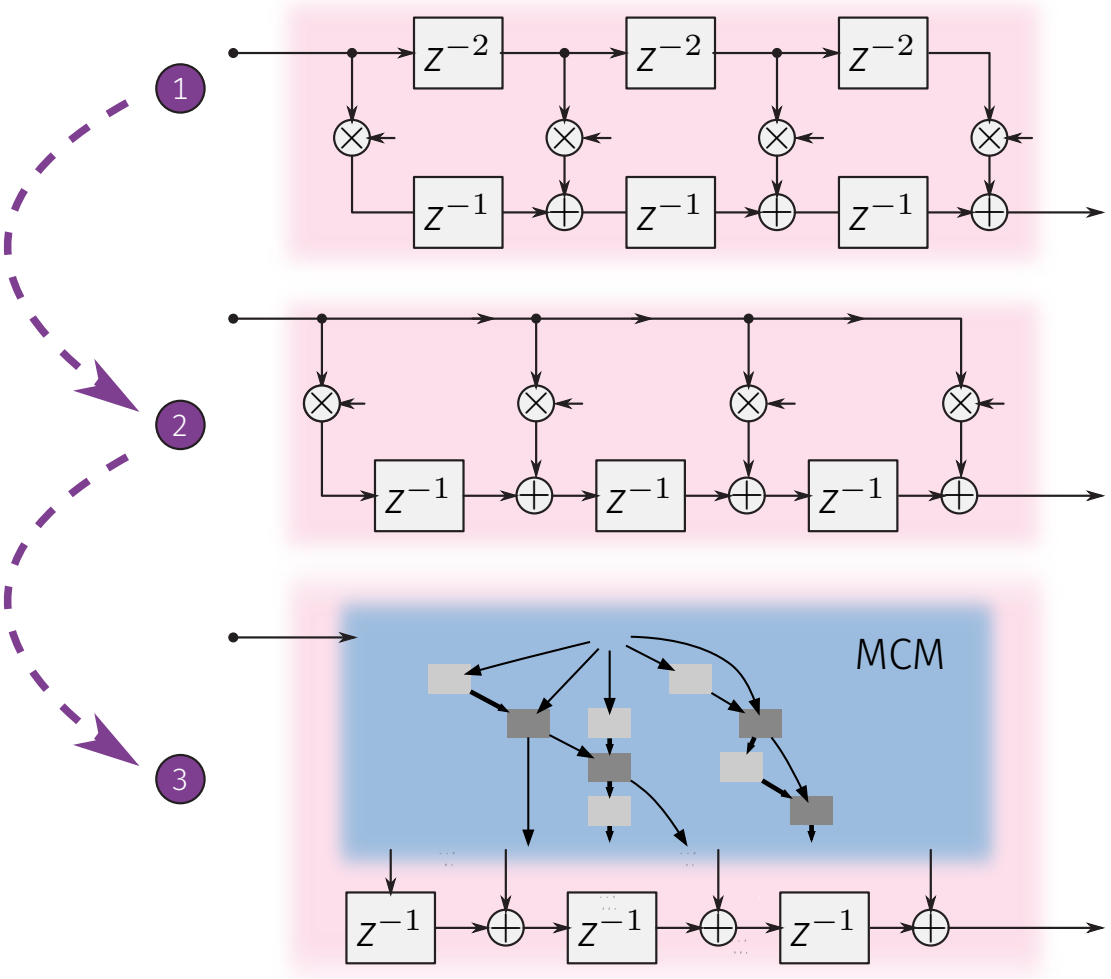


Let’s consider the front-end digital filters

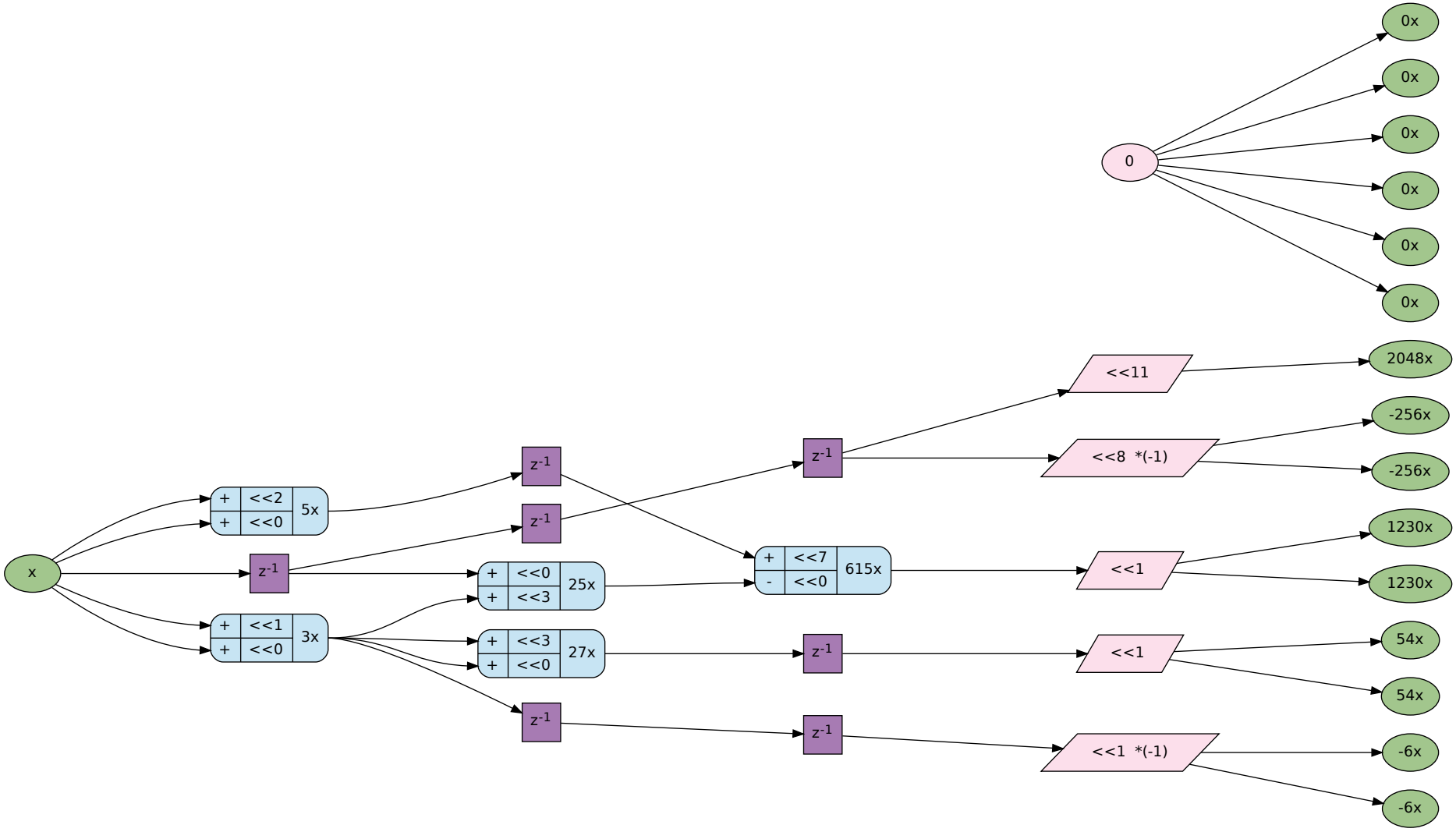
The Standard™ — Polyphase with DSP48 Multiply-Accumulates



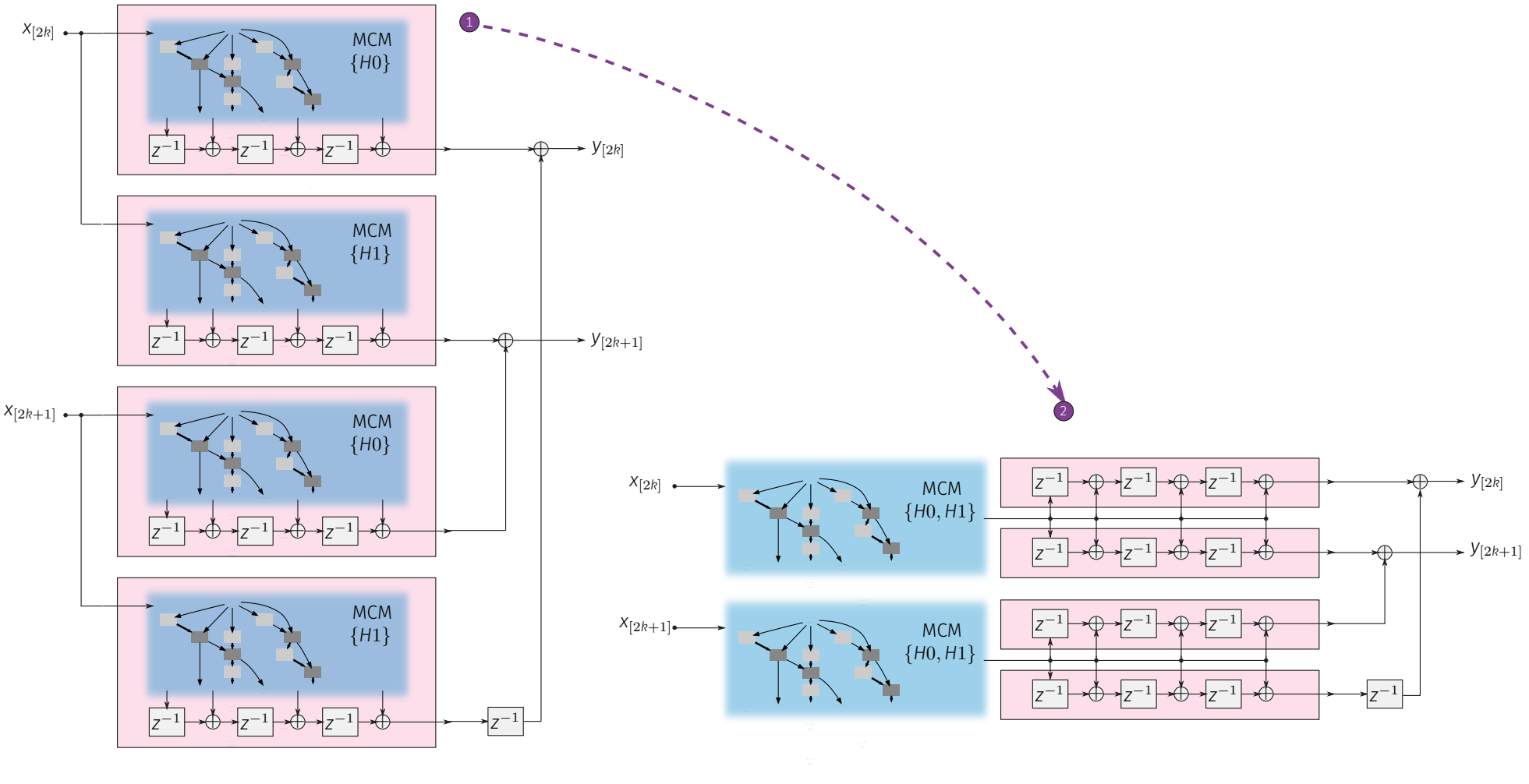
Optimising Subfilters — From Systolic to Multiplierless



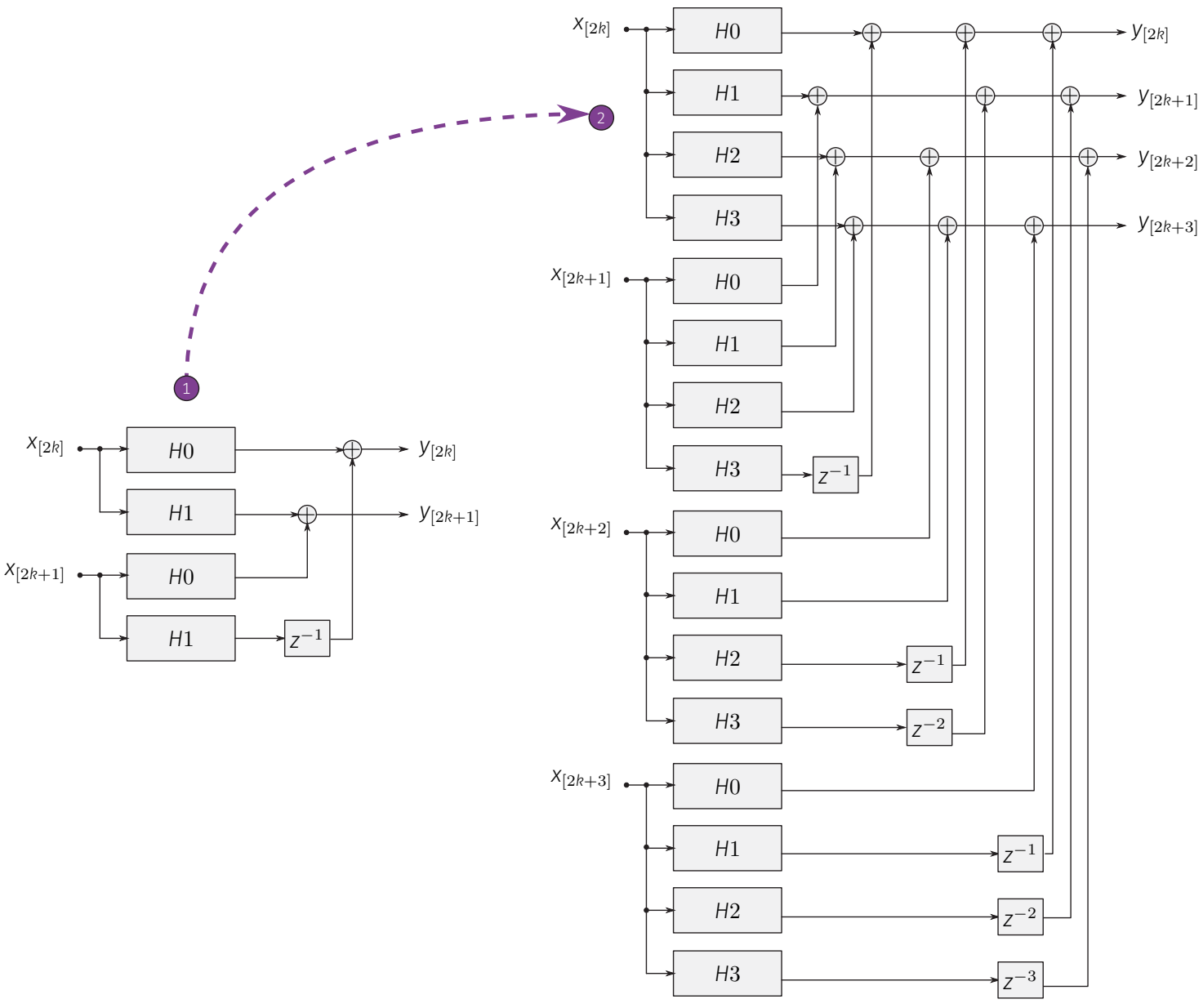
MCM Multiplier Blocks



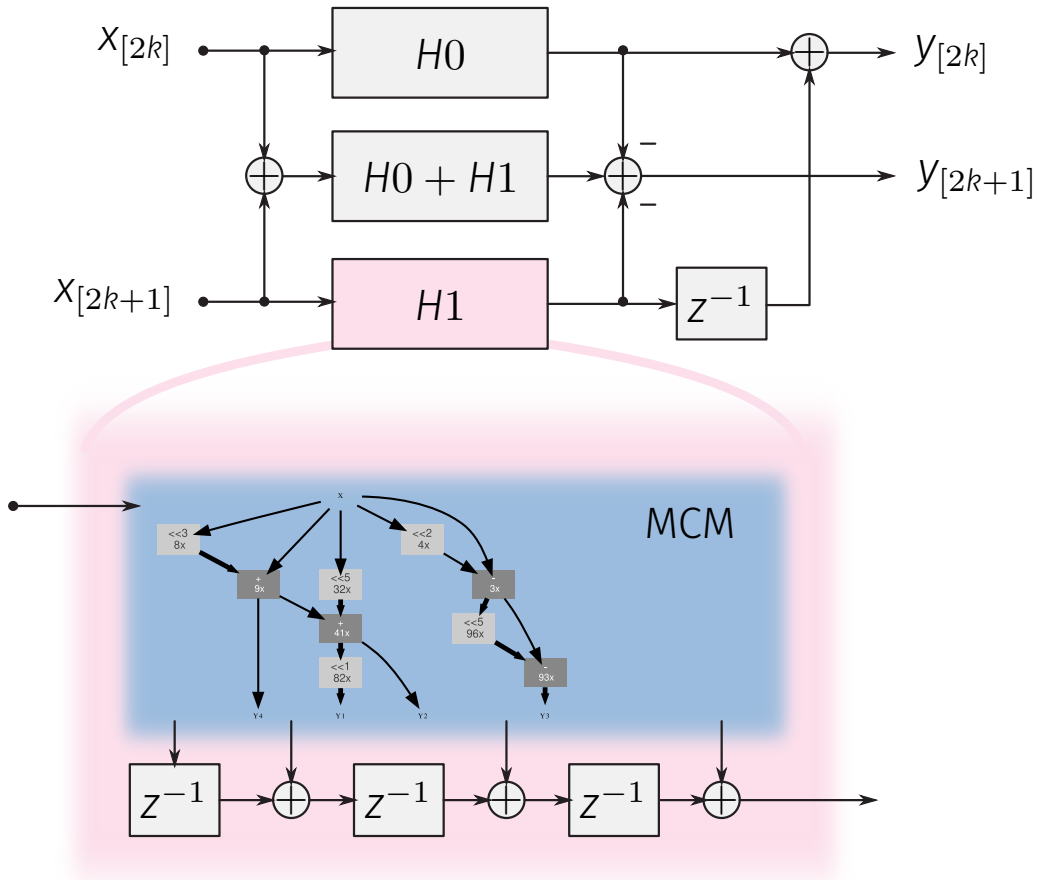
Optimising Parallelism — Resource sharing with Polyphase



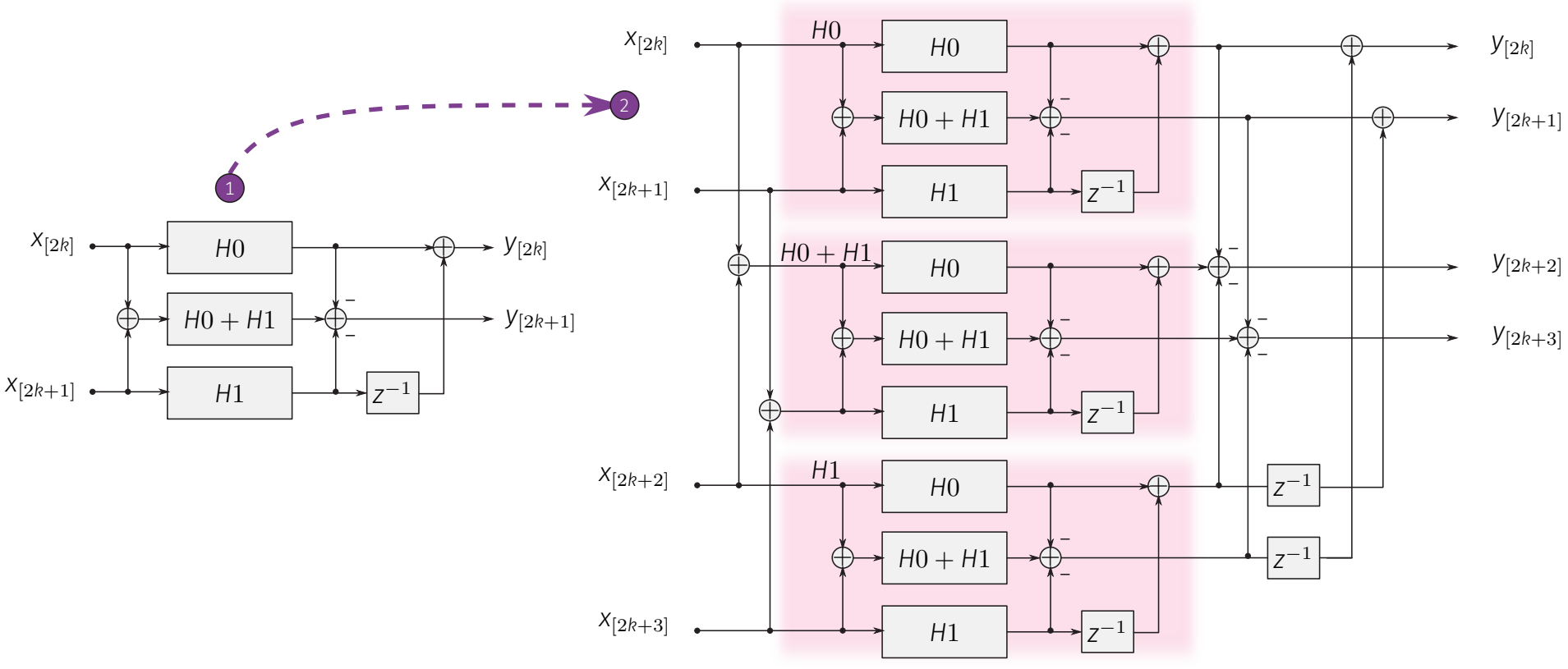
Scaling Parallelism — 4-parallel Polyphase



Proposed — FFA with MCM



Scaling Parallelism — 4-parallel FFA



Let’s consider the imacpt of

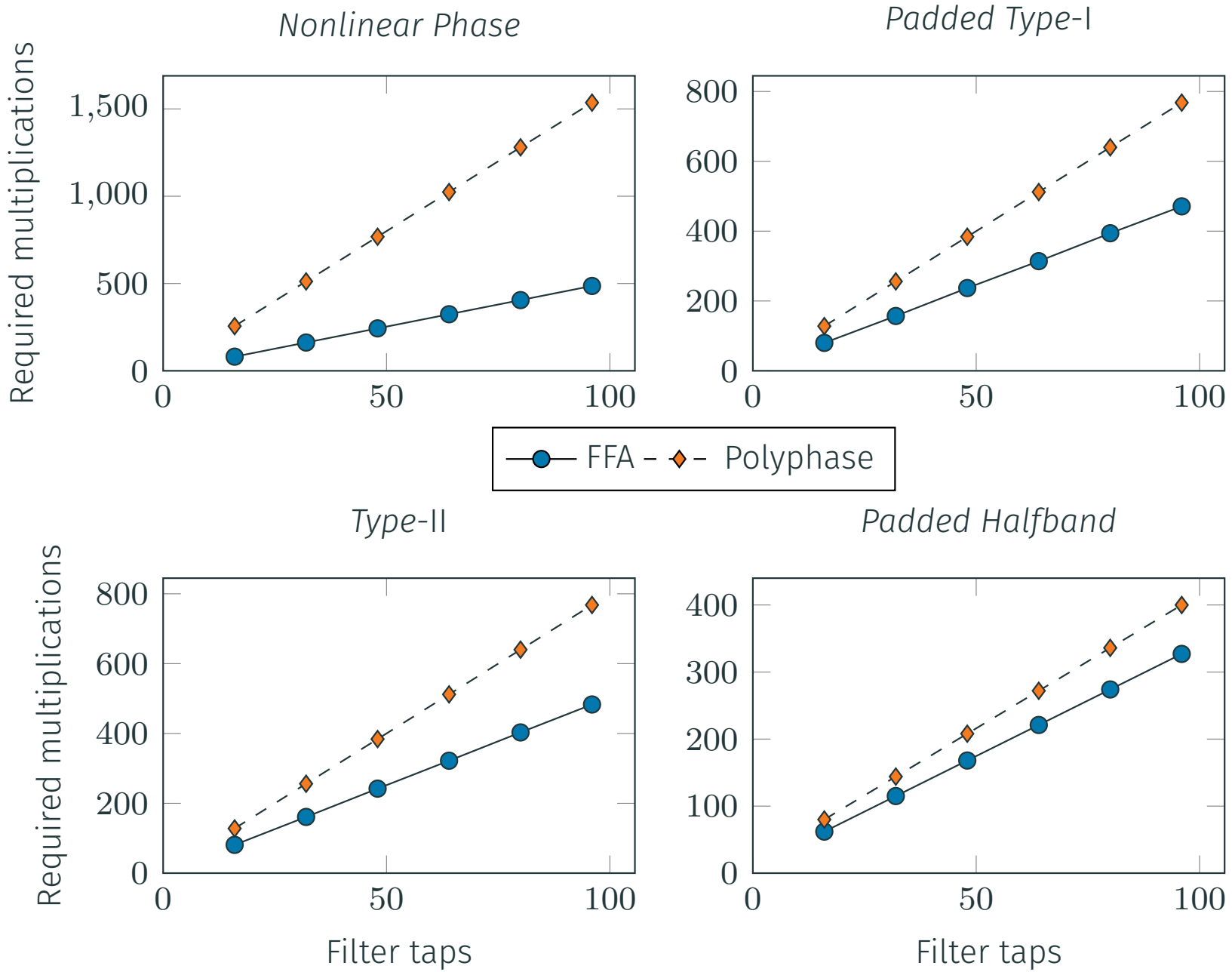
real-world coefficients

Coefficient Symmetry Summary

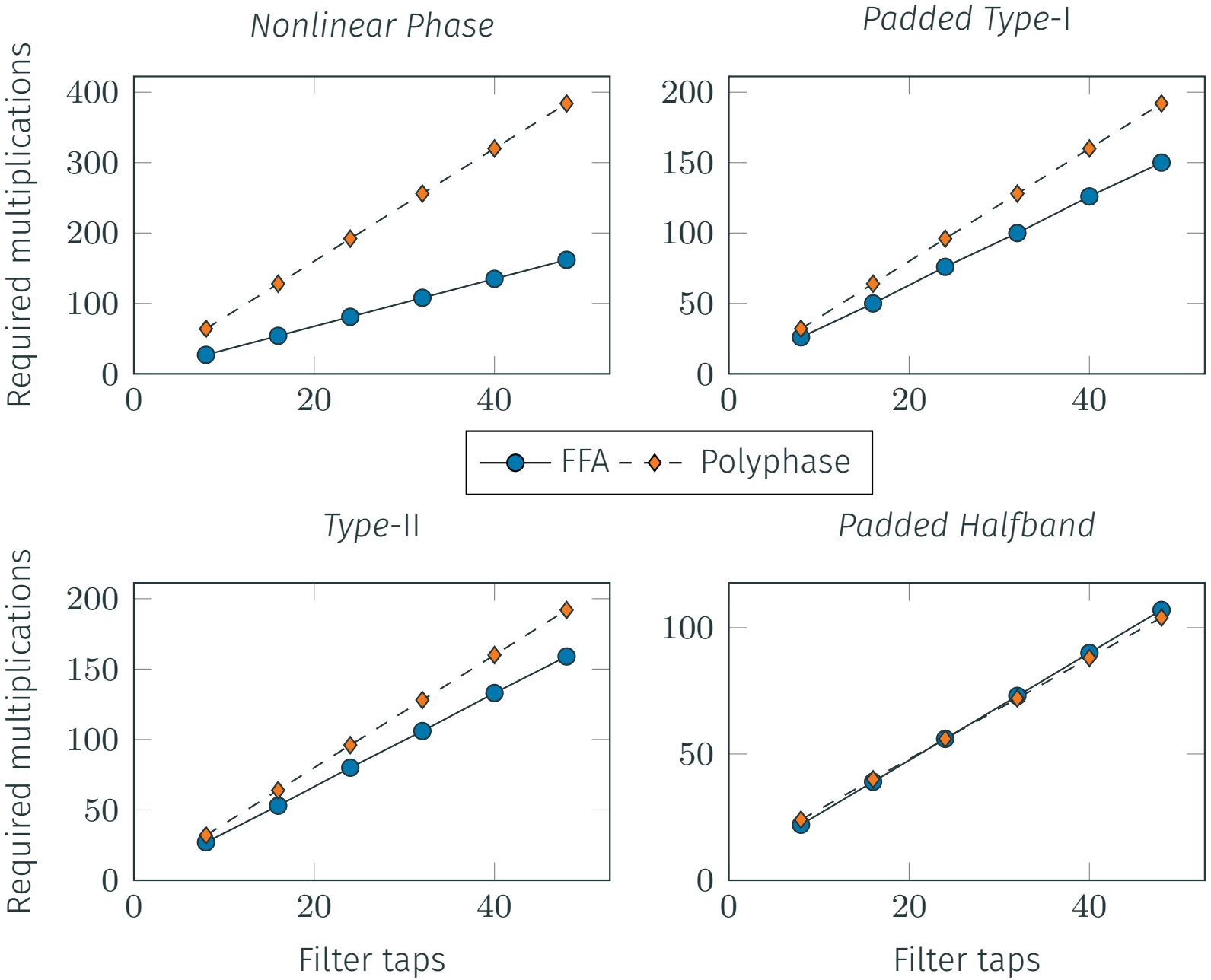
Multiplier cost for a 2^p-parallel filter with $2^p N$ weights is...

Coeffs	Polyphase	FFA
Nonlinear phase	$4^p N$	$3^p N$
Padded Type-I	$2^p \left\lceil \frac{2^p N}{2} \right\rceil$	$N(2 + \sum_{k=1}^{p-1} 3^k + 2 \sum_{i=0}^{p-2} \sum_{j=0}^{i} 3^j) + (p-1) \left\lceil \frac{N}{2} \right\rceil$
Type-II	$2^p \left\lfloor \frac{2^p N}{2} \right\rfloor$	$\left\lceil \frac{N}{2} \right\rceil + 2N \sum_{i=0}^{p-1} 3^i$
Padded Type-III	$2^p \left\lceil \frac{2^p N}{2} \right\rceil$	$N(2 + \sum_{k=1}^{p-1} 3^k + 2 \sum_{i=0}^{p-2} \sum_{j=0}^{i} 3^j) + (p-1) \left\lfloor \frac{N}{2} \right\rfloor$
Type-IV	$2^p \left\lfloor \frac{2^p N}{2} \right\rfloor$	$\left\lfloor \frac{N}{2} \right\rfloor + 2N \sum_{i=0}^{p-1} 3^i$
Half-band	$2^p \left\lceil \frac{2^p N}{4} \right\rceil$	$1 + 2^{p-1} + N + 4N \sum_{i=0}^{p-2} 3^i$

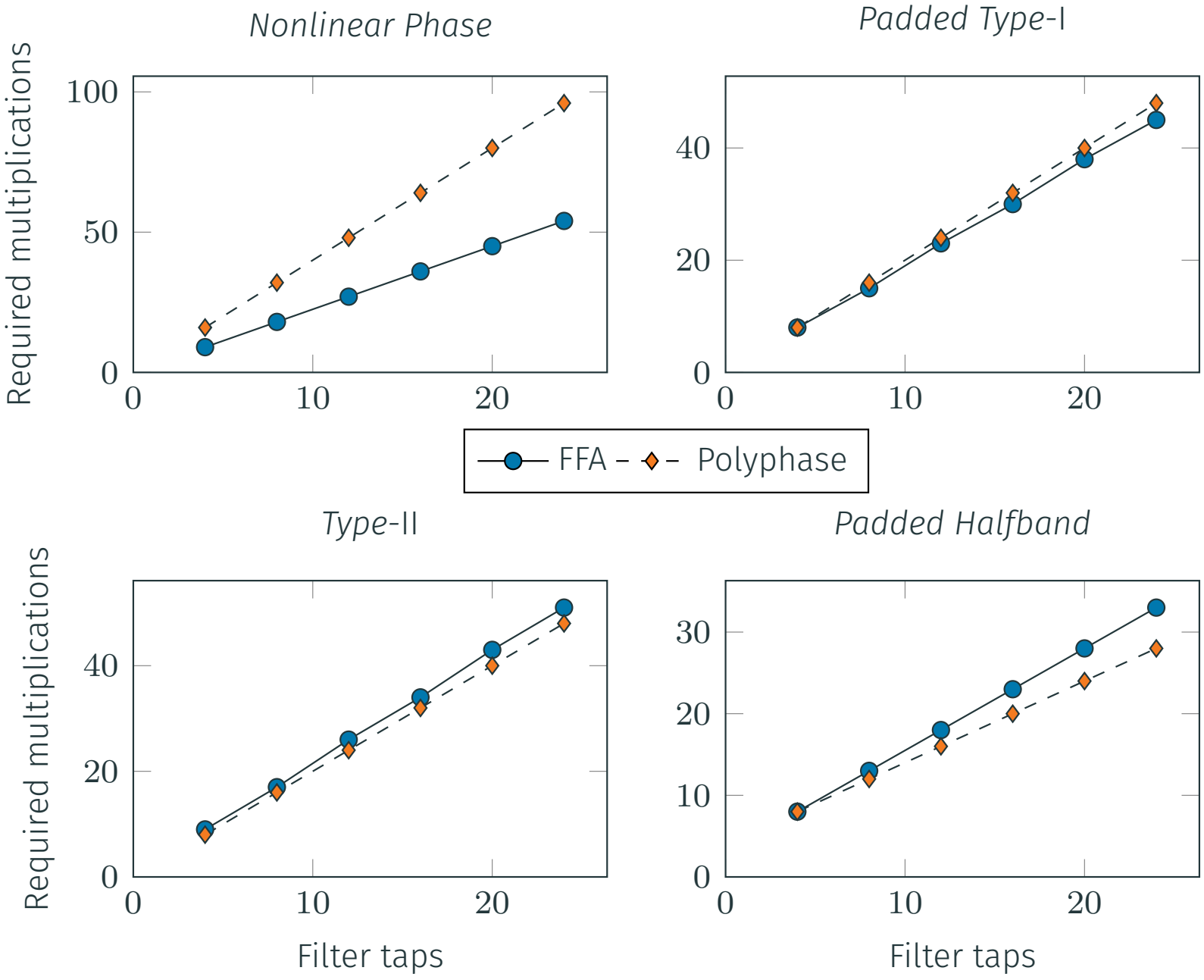
Realistic Unique Fundamentals — x16 Parallelism



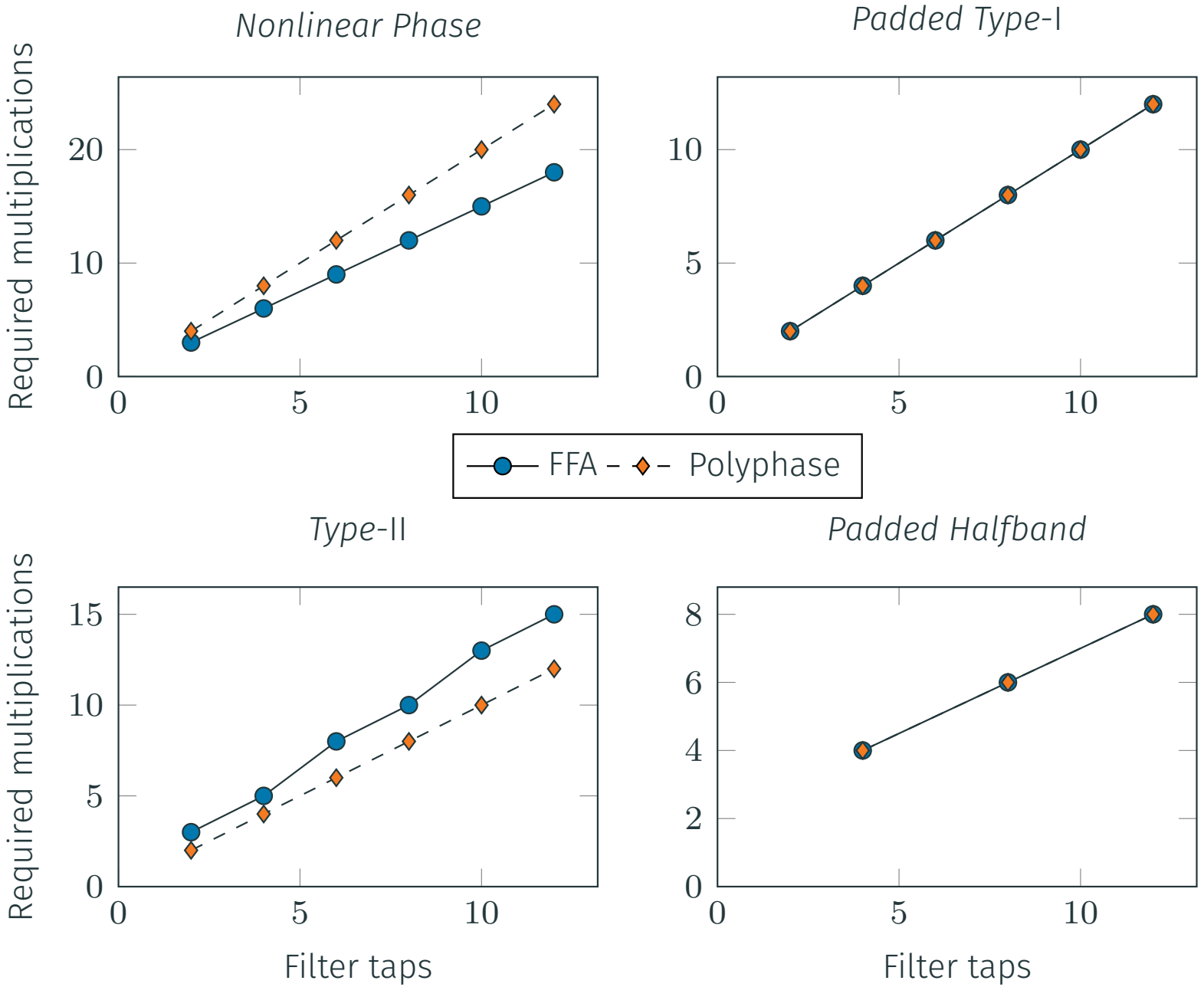
Realistic Unique Fundamentals — x8 Parallelism



Realistic Unique Fundamentals — x4 Parallelism

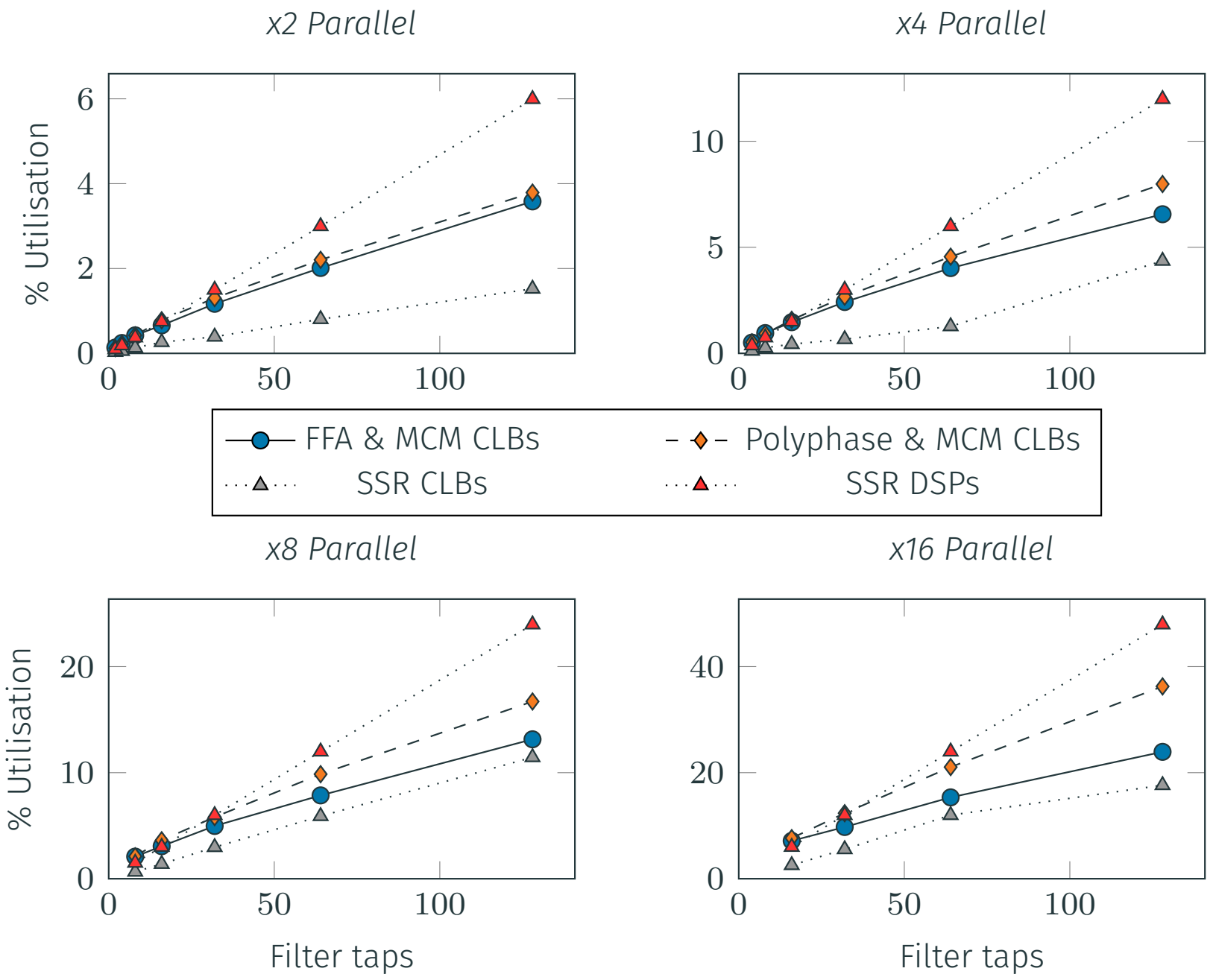


Realistic Unique Fundamentals — x2 Parallelism

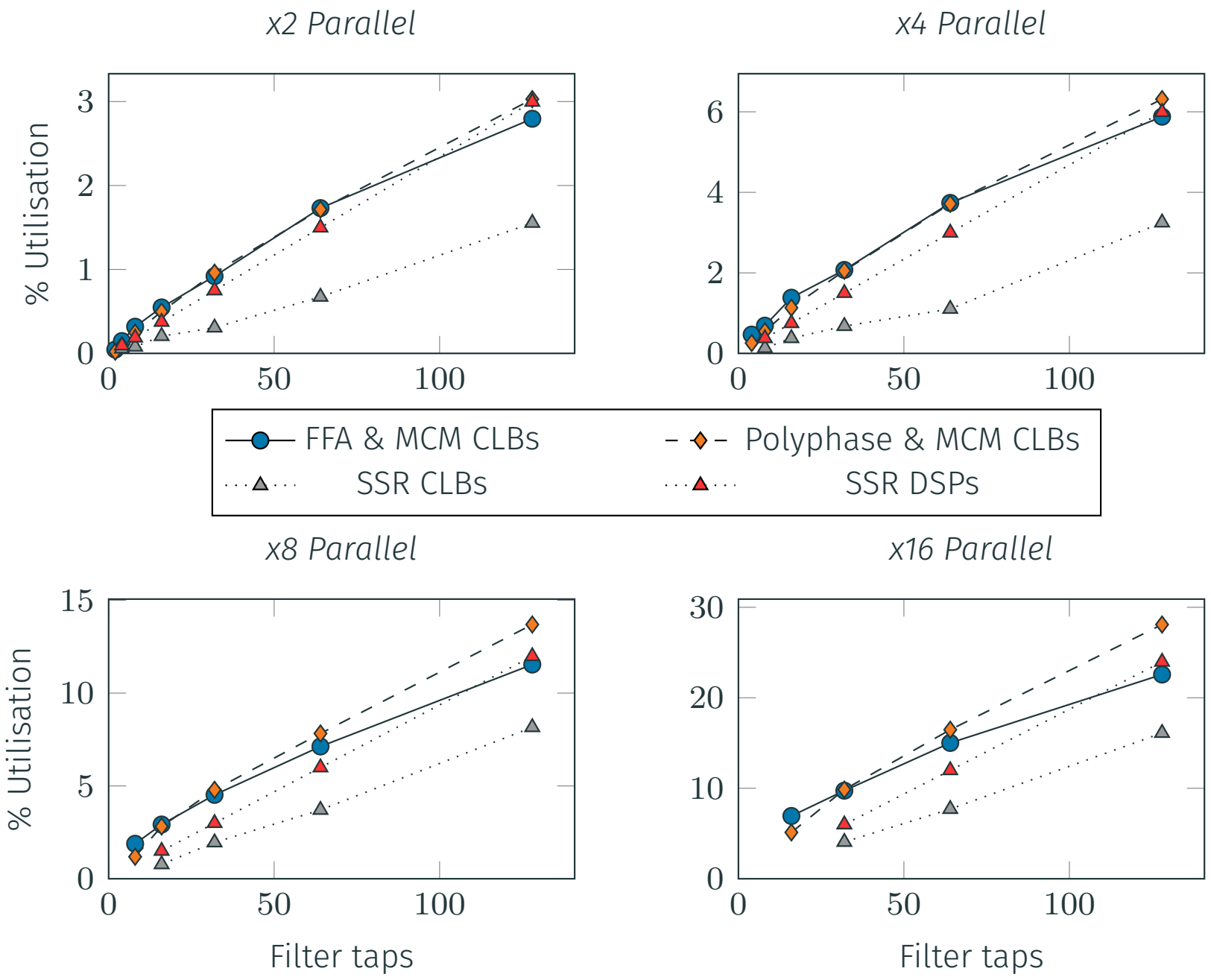


Implementation Results — Utilisation

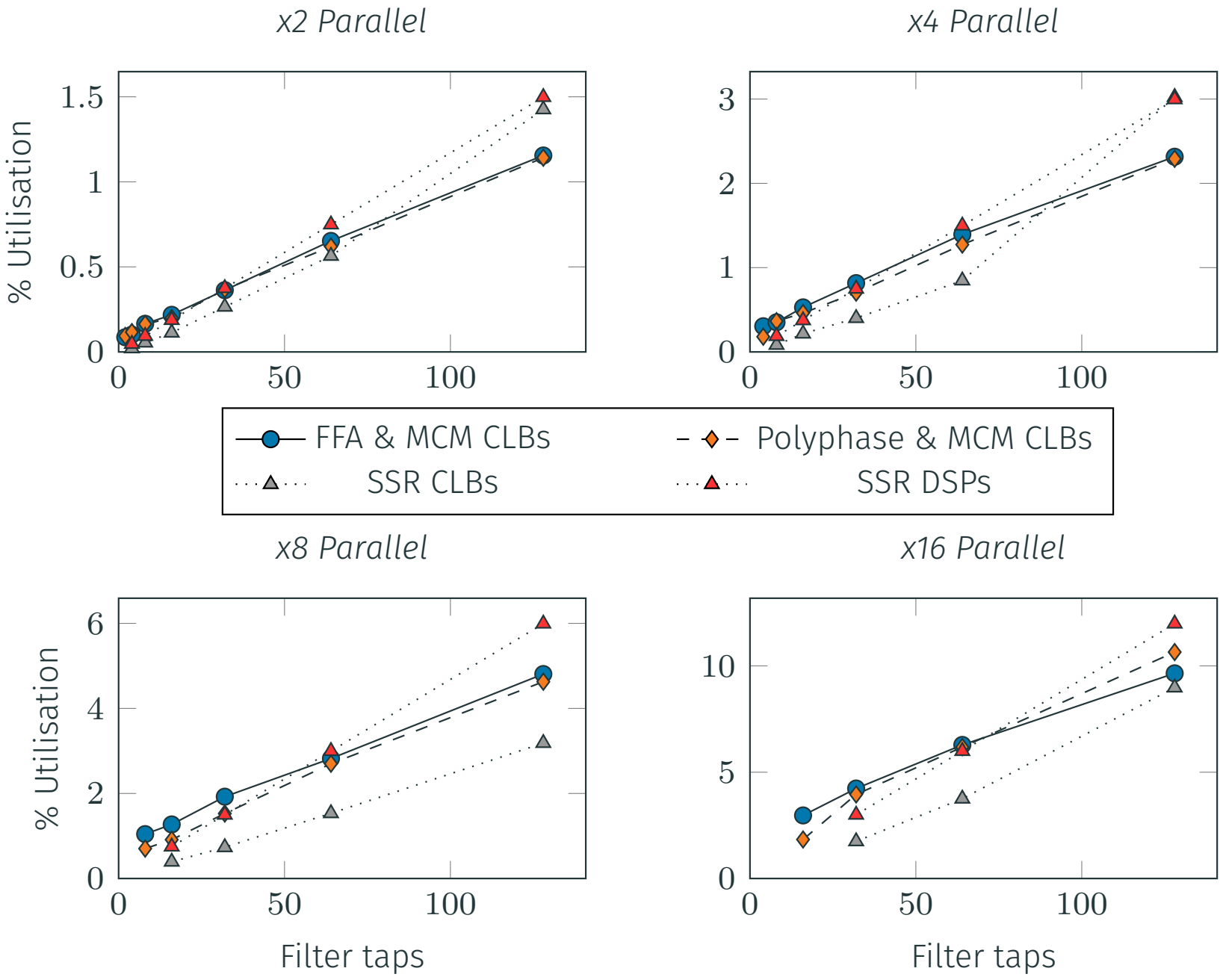
Implementation results — Nonlinear Phase Response



Implementation results — Padded Type-1 Response

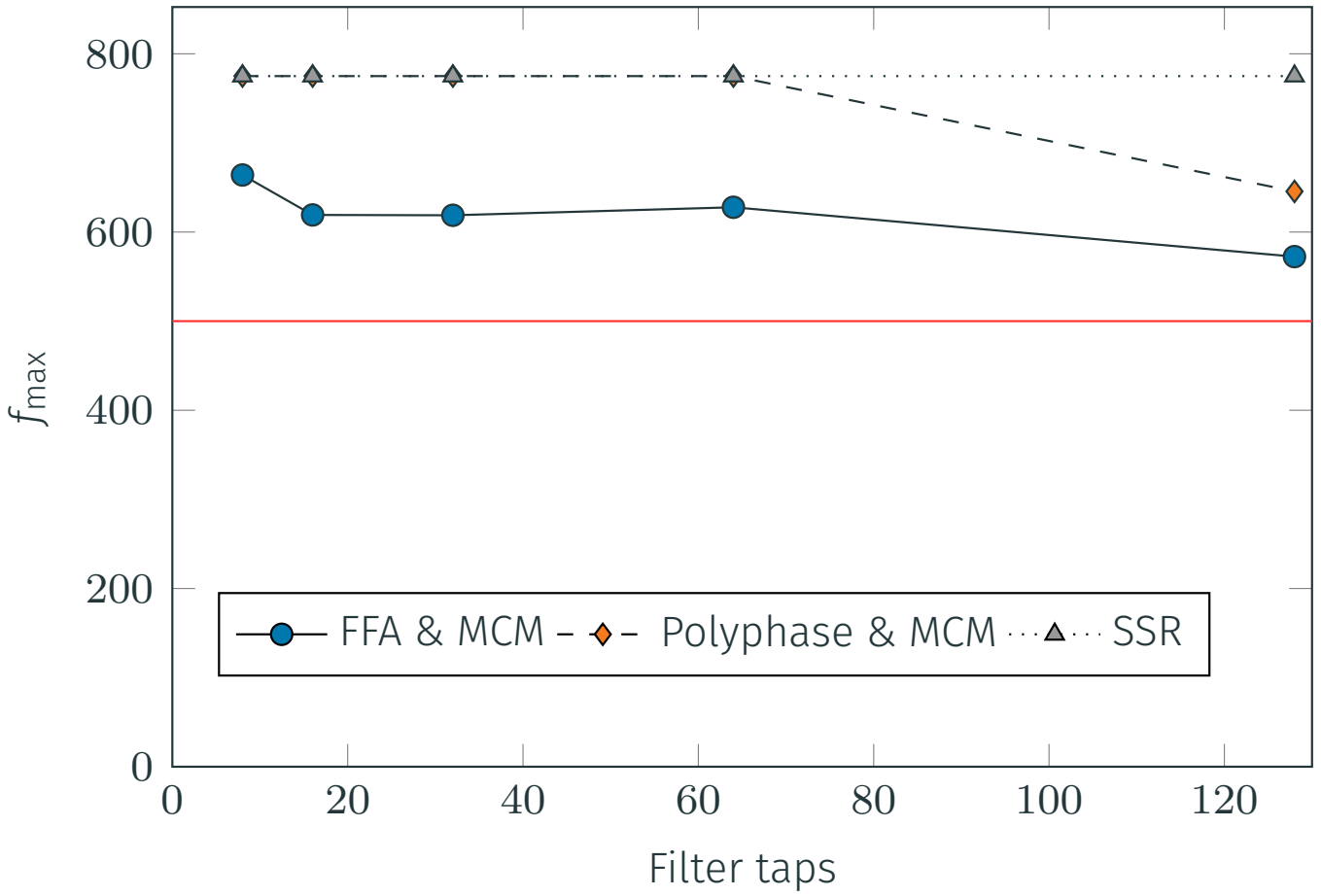


Implementation results — Halfband Response



Implementation Results — Frequency

f_{max} Estimates for x8 Parallel Half-bands



Language design and tooling

~~Language design and tooling~~

Conclusions

- Open source implementation of two new multiplierless filter constructs, with composition enabled by CλaSH
- Formal analysis of cost given real-world coefficient patterns common in RFSoC applications
- Comments on future language design to encourage similar future circuits
- ...Please take & modify these sources in academia and education! (*Contact us for commercial uses*)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